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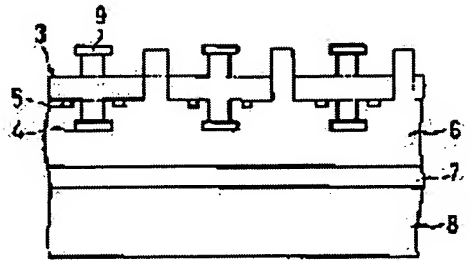
MORITSUKA KOHEI

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To manufacture efficiently a semiconductor device having a small parasitic capacitance, high reliability and high heat resistance.

SOLUTION: In a semiconductor device, semiconductor elements formed out of III-V compound semiconductor in each of which the widths of the active regions of its emitter and collector are smaller than the one of its base are provided in a body on a substrate 8 made of a different kind of material from them. In the semiconductor device, a semiconductor material 3 is divided into a plurality of small scattered portions for constituting the semiconductor elements, being covered with an insulator layer 6 to be prevented from abutting against the substrate 8. Forming from one side the insulator layer 6 covering the semiconductor material 3 subjected to a mold processing, the insulator layer 6 is heated to 300-400°C to join the substrate 8 to it.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by being formed with an III-V group compound and preparing a semiconductor device with the width of face of the active region of an emitter and a collector smaller than the active region of the base in one on the substrate of a dissimilar material.
[Claim 2] The semiconductor device which has a wrap insulator for this semi-conductor laminated material so that the elements of the semi-conductor laminated material subdivided by the element which constitutes 1 or two or more semiconductor devices, and this semi-conductor laminated material may be scattered and a substrate may not be touched.
[Claim 3] Carry out the laminating of the semi-conductor laminated material for forming a semiconductor device on the 1st substrate, and processing for fabricating this semi-conductor laminated material to a semiconductor device is performed to this semi-conductor laminated material from a said 1st substrate and opposite side. It joins forming the insulator layer which covers the processed part of this semi-conductor laminated material, and heating this insulator layer and the 2nd substrate at 300-400 degrees C. The manufacture approach of the semiconductor device characterized by separating said 1st substrate from this semi-conductor laminated material, performing a fabricating operation to this semi-conductor laminated material from a said 2nd substrate and opposite side, and making a semiconductor device complete this semi-conductor laminated material.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the heterojunction bipolar transistor IC by the III-V group compound semiconductor more about a semiconductor device and its manufacture approach at a detail.
[0002]
[Description of the Prior Art] Since an III-V group compound semiconductor device is in dominance in the point of electron mobility which the ingredient itself has compared with a silicon device, development as a ultra high-speed electron device is furthered, and it has an AlGaAs/GaAs heterojunction bipolar transistor etc. as the example. Since the emitter base junction of a heterojunction bipolar transistor (Following HBT is called) is formed by the heterojunction, it is possible to make high impurity concentration of a base region sufficiently high, and to lower base resistance, without making high impurity concentration of an emitter into high concentration, and it excels in the RF property. Therefore, development is furthered as a transistor for microwave etc.
[0003] As an index of the working speed of a bipolar transistor, it is a cut off frequency ft. And maximum oscillation frequency fmax It is. general -- cut off frequency ft Emitter depletion-layer charging-time tauE and base-transit-time tauB and collector depletion-layer transit-time tauX And collector charging-time tauC from -- it is expressed with a degree type (1) and (2).
ft =1/(2pitauEC) (1)
tau EC=tau E+tauB+tauX+tauC (2)
[0004] moreover, maximum oscillation frequency fmax Base resistance RB, the collector junction capacity CCB, and the above-mentioned cut off frequency ft from -- it is expressed with the following type (3).
fmax =ft/(8piRB CCB) (3)
[0005] maximum oscillation frequency fmax in order to make it high -- cut off frequency ft high -- carrying out -- further -- base resistance RB and the collector junction capacity CCB -- small -- it is necessary to carry out -- cut off frequency ft In order to make it high, it is necessary to shorten the transit time in a component of a carrier. And it is base-transit-time tauB as what is considered in order to shorten the transit time in a component of a carrier. There is compaction. Base-transit-time tauB It is base resistance RB as it will be shortened if base width of face is made small, but sheet resistance will increase twice, if base width of face is set to one half. Since it increases, it is base resistance RB. Even if it changes, it is maximum oscillation frequency fmax as a result. Improvement is not expectable. There is the approach of reducing by extending the depletion-layer width of face between base collectors, or on the other hand, reducing the area between base collectors about the collector junction capacity Ccb. The collector transit time increases by the approach of extending the former depletion-layer width of face, and it is a cut off frequency ft. It falls. Although the approach of arranging a collector to the up side and using as the collector top mold HBT as an approach of reducing the area between the latter base collectors etc. is developed, in the case of this structure, the leakage current between the emitter

collectors separated by ion implantation is large, and there is a problem from which a high current amplification factor is not obtained. Moreover, it sets in the emitter top mold HBT, and is H+ because of the collector parasitic capacitance reduction under the external base. Or O+ The implantation using ion is used. A collector non-intrinsic region depletion-izes with this technique, and collector parasitic capacitance is reduced. However, if the parasitic capacitance between a collector contact layer and an external base layer still remains and this parasitic capacitance is not eliminated, the further improvement in the speed is difficult.

[0006] On the other hand, the United States patent official report No. 5,318,916 The approach of producing HBT using an epitaxial lift off is indicated. By this approach The semi-conductor laminating thin film formed on the 1st substrate Shaping processing by the side of an emitter is performed by processing from this substrate side and an opposite side, after this, the 2nd substrate is stuck on the emitter side of a processing thin film, selective etching removes the 1st substrate, a laminating thin film is again processed from the side exposed by this, and shaping by the side of a collector is performed. According to this approach, it becomes possible to process it so that collector parasitic capacitance may be reduced at the time of processing by the side of a collector, and to produce ultra high-speed HBT.

[0007]

[Problem(s) to be Solved by the Invention] However, if HBT is produced using an above-mentioned approach, in the mass production using production of IC, or the wafer of a large area, various failures will arise.

[0008] For example, a laminating thin film tends to cause exfoliation and destruction with the stress concerning the emitter side of the laminating thin film stuck on the 2nd substrate by the heat imposed into a subsequent process.

[0009] Moreover, if the 2nd substrate is stuck by the adhesion approach by the adhesives metallurgy group, since it will be easy to produce a void into a covering part and dispersion in a device property will become large by the void, inconvenience is produced in severe IC production of the demand to the homogeneity of a device property.

[0010] Furthermore, the metal on which the 2nd substrate and laminating thin film are pasted up in the above-mentioned production approach is as common as an emitter metal or a collector metal, and since only the circuit of a grounded emitter or the circuit of a grounded collector can be formed in this configuration, the application to IC design is restricted.

[0011] If a device with little parasitic capacitance is produced in order to accelerate actuation of a bipolar transistor according to the conventional approach so that I may be understood from the above-mentioned explanation, productive efficiency is low and the high device of dependability and thermal resistance cannot be obtained. Therefore, in order to raise productive efficiency, the dependability of a device, and thermal resistance, prevention of breakage of the laminating thin film resulting from the void and thermal stress of a junction interface with a semi-conductor substrate is an important technical problem.

[0012]

[Means for Solving the Problem] In order to attain the above-mentioned object, as a result of inquiring about device structure or a device fabrication process, by devising the configuration of the laminating thin film and substrate which constitute a transistor component, breakage of the laminating thin film by thermal stress is decreased, and it came to accomplish a header and this invention for the ability of the effect of the void of a junction interface to be mitigated by thermal processing in a fabrication process.

[0013] The semiconductor device of this invention is formed with an III-V group compound, and a semiconductor device with the width of face of the active region of an emitter and a collector smaller than the active region of the base is prepared in one on the substrate of a dissimilar material.

[0014] Moreover, the semiconductor device of this invention has a wrap insulator for this semi-conductor laminated material so that the elements of the semi-conductor laminated material subdivided by the element which constitutes 1 or two or more semiconductor devices, and this semi-conductor laminated material may be scattered and a substrate may not be touched.

[0015] Furthermore, the manufacture approach of the semiconductor device of this invention Carry out

the laminating of the semi-conductor laminated material for forming a semiconductor device on the 1st substrate, and processing for fabricating this semi-conductor laminated material to a semiconductor device is performed to this semi-conductor laminated material from a said 1st substrate and opposite side. It joins forming the insulator layer which covers the processed part of this semi-conductor laminated material, and heating this insulator layer and the 2nd substrate at 300-400 degrees C. Said 1st substrate is separated from this semi-conductor laminated material, a fabricating operation is performed to this semi-conductor laminated material from a said 2nd substrate and opposite side, and a semiconductor device is made to complete this semi-conductor laminated material.

[0016] According to the above-mentioned configuration, breakage of thermal stress or the semi-conductor laminated material by heating expansion of a void is prevented, the thermal resistance of a semiconductor device and dependability are improved by this, and the productive efficiency in a production process is improved.

[0017]

[Embodiment of the Invention] The outline of a fabrication of the semiconductor device concerning this invention is explained below with reference to a drawing. In a drawing, (B) of the vertical section of a semiconductor device [in / in (A) and drawing 7 of drawing 1 -5 and drawing 6 / a fabrication process] and drawing 6 is the top view of the device of (A) of drawing 6 .

[0018] First, epitaxial growth of the selective etching layer 2 is carried out on the 1st substrate 1, i.e., a semi-conductor substrate, the semi-conductor thin film laminating 3 for forming an emitter, the base, and a collector is formed on it, and as etching processing is carried out from a substrate 1 and opposite side and this semi-conductor thin film laminating 3 is shown in drawing 1 , the emitter electrode 4, a base electrode 5, and a wiring electrode (not shown) are prepared. Then, like drawing 2 , it etches so that the semi-conductor thin film laminating 3 may be divided into each element. And the wrap insulator layer 6 is formed for the semi-conductor thin film laminating 3 etched like drawing 3 so that a top face might become flat over the whole substrate surface. The insulator layer 6 is formed by polyimide resin, the polymer of benz-cyclo-butene (BCB), etc. Then, the laminating of a wiring electrode and the insulator layer is carried out if needed, and a multilayer interconnection is formed (not shown). Next, the metal layer 7 is formed on the insulator layer 6 (or multilayer interconnection) like drawing 4 , this metal layer 7 and the 2nd substrate 8, i.e., a support substrate, are pasted up, and the upper and lower sides are reversed like drawing 5 . Adhesion with the metal layer 7 and the support substrate 8 can be performed using alloying with the metal layer 7 and the support substrate 8, using adhesives. When using adhesives, it is desirable to have resistance to an about 400-degree C elevated temperature, and for adhesives strong also against an acid to be applied, and to heat the support substrate 8 and the metal layer 7 at about 300-400 degrees C at the time of adhesion. When pasting up by alloying, it alloys at the temperature of about 300-400 degrees C. Usually, if a void is in an adhesion interface, when a substrate is heated in down stream processing of the substrate after adhesion, destruction of a device will take place by expansion and explosion of the gas in a void. However, prevention of device destruction of after that resulting from a void is attained by adhesion accompanied by about 400-degree C heating as mentioned above. As adhesives suitable for an activity, adhesives, such as polyimide resin and an epoxy resin, are mentioned, for example. Although metal simple substances, such as Pt, Pd, Ti, and nickel, can be used for the metal layer 7, metal laminated material like not only these but Ti/Pt/Au/Pt/Ti/Pt or Ti/Pt/Au/Pt/Ti/Pd may be used. In addition, it is possible to choose suitably if needed with a conventional method about the construction material of a wiring electrode, for example, to use Ti/Pt/Au etc. When pasting up the 2nd substrate with adhesives, and the substrate which has irregularity in a front face is used, it is desirable in respect of bond strength.

[0019] Then, by etching the selective etching layer 2 and removing the semi-conductor substrate 1, as shown in (A) of drawing 6 , the semi-conductor thin film laminating 3 is put. At this time, the semi-conductor thin film laminating 3 exposed to a top face in the shape of a rectangle as shown in (B) of drawing 6 is the part of a collector layer, and peeling and breakage by thermal stress are prevented by dividing the semi-conductor thin film laminating 3 into many elements in this way. As shown in drawing 7 , the exposed semi-conductor thin film laminating 3 makes a collector field small by etching,

in order to decrease the parasitic capacitance of a collector layer. Under the present circumstances, in order to lower base contact resistance, it may etch until a base layer is exposed, and a base electrode may be formed. A collector electrode 9 is formed in the semi-conductor thin film laminating 3 after etching like drawing 7 . Then, wiring needed by pulling out wiring which covers with an insulator layer and is formed in the bottom of the semi-conductor thin film laminating 3 on the front face of the 2nd substrate and an opposite hand with a conventional method is performed. In production of IC, wiring between the elements of the divided semi-conductor thin film laminating 3 is performed.

[0020] The width of face of an emitter and a collector is quite smaller than the width of face of the base inserted into these, and it consists of symmetrically vertical mold bipolar transistors produced as mentioned above with an emitter to the base so that it may be set to about 1 / 4 - 1/2 of the width of face of the base (it is about 0.5-2 micrometers as an emitter and collector width of face). The collector which parasitic capacitance becomes small since the width of face of the active region of an emitter and a collector becomes smaller than the base by this, and consists only of an intrinsic region substantially used for originally a current flowing can be obtained. Moreover, base contact resistance also becomes small. For example, it is fmax if collector capacitance is decreased to one half according to the above-mentioned configuration under the conditions whose base width of face is 1 micrometer and whose emitter width of face is 2 micrometers. The efficiency of improving from 170GHz to 220GHz is obtained.

[0021] When a substrate and a semi-conductor thin film laminating are the conventional semiconductor devices joined directly, and a device is heated, with the stress produced according to the difference of the coefficient of thermal expansion of a substrate and a semi-conductor part, a semi-conductor thin film laminating exfoliates from a substrate, or is damaged. Since the operation gestalt of stress is also the same as when joined through the metal layer, the same is substantially [as what is directly joined to the substrate] said of such a thing. However, in the semiconductor device of this invention, since a semi-conductor thin film laminating part separates from a substrate and is joined through the insulator, such stress acts on an insulator. Furthermore, unlike the case where, as for the operation gestalt of the stress produced between an insulator and a semi-conductor thin film laminating, the semi-conductor thin film laminating is joined to the substrate since the semi-conductor thin film laminating is formed so that it may be subdivided by the element and may be covered with an insulator, breakage of the semi-conductor thin film laminating by thermal stress is controlled. Moreover, there is no failure in joining a different-species substrate like thermally conductive good alumimium nitride.

[0022] The magnitude with the suitable element of semi-conductor thin film **** is called for as follows. If the device embedded at the insulator after the semi-conductor which die length of one side has the base of the square of w, and was temporarily subdivided by the element of the rectangular parallelepiped form where thickness is d had put the top face of the square outside is assumed When a device is heated, with the thermal stress sigma produced to a semi-conductor, a semi-conductor receives bending stress from an insulator, and if sigma' is small in the buckling strength of a semi-conductor, a semi-conductor will exfoliate from an insulator, without the ability bearing bending stress. The thermal stress sigma produced to a semi-conductor is expressed with the following formula (1), and, on the other hand, sigma' is expressed with the following formula (2) according to the formula of an oiler from minimum second-moment-of-area [of a semi-conductor] I, and the minimum radius of gyration of area k in buckling strength.

Sigma=E-alpha-deltat (1)

(However, inside of a formula and E an elastic modulus and alpha coefficient of linear expansion and deltat temperature change)

I=wd3 / 12 k2 =d2 / 12 sigma'= n-pi 2 and E-d2 / 12w2 (2)

(The inside of a formula and n are a terminal multiplier)

[0023] Since exfoliation of a semi-conductor is not produced when buckling strength and thermal stress are set to sigma'>2sigma, die-length [of one side] w and thickness d which fulfill this condition have a relation like the following formula (3) from the above-mentioned formula (1) and (2).

w< [[(n-pi 2)]/[/] (24alpha-deltat)] 1/2, and d (3)

[0024] Therefore, exfoliation will not be produced if die-length [of one side] w is set as the value with which are satisfied of the above-mentioned formula (3) on the basis of thickness d of an element. For example, when a semi-conductor is GaAs, coefficient of linear expansion alpha is 6x10-6/K, and if it carries out to d= 2 micrometers in the terminal multiplier n= 1, temperature-change deltat=300K, and thickness, die-length [of one side] w will be set to less than 30 micrometers.
[0025] Breakage of the semi-conductor thin film laminating by thermal stress can be decreased by making it the structure which subdivided the semi-conductor thin film laminating in the element, and was embedded in the insulator layer so that I may be understood from ****. That what is necessary is just to set the magnitude of each element as the range drawn with reference to above-mentioned requirements according to each situation, an element may be formed in component units, such as a transistor, or may form two or more components as one group. About an insulator, it is required to have the reinforcement which can bear the stress of extent put under heating, and an ingredient which was mentioned above as an example of an insulator satisfies this.
[0026] Furthermore, the heat produced from a transistor is efficiently emitted outside from a substrate by preparing a laminating part in a metal layer between a wrap insulator and the 2nd substrate. It is also possible to connect wiring for heat dissipation to a metal layer from a transistor.
[0027] Moreover, if an insulator has sufficiently high reinforcement, it is also possible to form the 2nd substrate with an insulator. That is, a part of insulator layer serves as substitution of a substrate, and the 2nd substrate is omitted. Polyimide resin is excellent in such a mode especially as an insulator.
[0028] Although production of the transistor of a collector top mold is described in the above-mentioned explanation, to say nothing of the ability to also produce an emitter top mold, it is applicable about other components.
[0029] The example of production of the semiconductor device concerning this invention is mixed with below, and a drawing is explained to it for it at a detail. in addition -- the crystal growth approach -- MOCVD -- law and MBE -- law and the gas source MBE -- although there is law etc. -- here -- MBE -- it shall carry out by law
[0030] As a selective etching layer 12 on the half-insulation GaAs substrate 11 as shown in drawing 8 (Example 1) An InGaP layer with a thickness of 1 micrometer An n+-GaAs layer as a collector layer 14 as a collector contact layer 13 a 400nm n-GaAs layer As a base layer 15, a 45nm P+-Alx Ga1-x As layer (x= 0->0.1) Crystal growth of the 50nm n+-In0.5 Ga0.5 As layer is carried out one by one as an emitter layer 16 as a 100nm N-aluminum0.3 Ga0.7 As layer and an emitter contact layer 17, and laminated material is obtained.
[0031] Next, it is B+ as the slanting broken-line part I shows parts other than the part which serves as a component among laminated material to drawing 9 , in order to classify laminated material for every component. The ion implantation in ion is performed. Then, by etching using the mixed liquor of phosphoric acid and a hydrogen peroxide, parts other than the emitter region in an emitter contact layer and the emitter layer 16 are removed like drawing 10 , and the base layer 15 is exposed.
[0032] Furthermore, the emitter electrode 18 and a base electrode 19 are formed by Ti/Pt/Au with vacuum deposition like drawing 11 . And it divides into the element containing the part which etches laminated material in the shape of a grid, and serves as a component of a predetermined number like drawing 12 . It is made for the depth of etching to become deeper than the collector contact layer 13 at this time. Then, like drawing 13 , the insulator layer 20 which applies a polyimide precursor all over a substrate, is made to heat and carry out heat curing to 350 degrees C, and consists of polyimide resin is formed so that an element may be covered, and flattening is carried out with etchback.
[0033] And as shown in drawing 14 , a contact hole is opened in the polyimide resin of the upper part location of the emitter electrode 18 and a base electrode 19, the wiring 21 for each electrodes is formed by Ti/Pt/Au, and it covers with polyimide resin further, it heat-hardens similarly, and the insulator layer 22 is formed. Then, the whole front face of the insulator layer 22 of polyimide resin is made to vapor-deposit the platinum thin film 23 like drawing 15 , as shown in drawing 16 , a silicon substrate 24 is contacted to said platinum thin film 23, it heats at 350 degrees C, and a silicon substrate 24 is pasted up on the platinum thin film 23 by alloying of platinum and silicon.

[0034] Furthermore, as the selective etching layer 12 of InGaP is etched using a hydrochloric acid and it is shown in drawing 17 , the epitaxial lift off of the GaAs substrate 11 is carried out. In the condition of having removed the substrate 11, the laminating part which forms a component is divided into an element, and will be in the condition of having been been scattered and laid underground by Mr. Shima into the insulator layer 20 of polyimide resin, and since direct coupling of the substrate is not carried out, breakage of the component by the thermal stress produced by heat treatment performed henceforth stops being able to happen easily.
[0035] Then, like drawing 18 , etching removes the collector contact layers 13 and collector layers 14 other than the part which forms a collector field, the base layer 15 is exposed, and the base electrode 25 made from Ti/Pt/Au is attached with vacuum deposition so that a collector may become symmetrical with an emitter about the base. Similarly, a collector electrode 26 is attached to the collector contact layer 13. It becomes possible by forming base electrodes 19 and 25 in the vertical both sides of a base layer to decrease breadth contact resistance of contact area.
[0036] Furthermore, a top face is covered with benz-cyclo-butene (BCB), this is stiffened at 250 degrees C, flattening is carried out with etchback, and the insulator layer 27 is formed like drawing 19 . the collector electrode 26 from the top face of the insulator layer 27, a base electrode 25, and the lower layer wiring 21 -- going -- the direction of a vertical -- a contact hole -- forming -- wiring -- public funds -- Ti/Pt/Au is embedded as a group, the cash-drawer wiring 28 is formed, and a heterojunction bipolar transistor component is completed.
[0037] (Example 2) According to the same actuation as an example 1, as shown in drawing 20 , two or more transistor components 30 laid under the insulator layers 20, 22, and 27 are formed, each component 30 is further connected with the bilayer wiring 29, and IC31 is produced.
[0038] (Example 3) Actuation of an example 1 is applied and IC32 as shown in drawing 21 is produced. The heat which connected the emitter electrode 34 of the required component 33 for power of especially the cure against heat dissipation with the metal layer 23 with the wiring 35 made from Au among transistor components, and was produced for the component 33 in this IC is made easy to transmit to the metal layer 23 through wiring 35.
[0039] (Example 4) Actuation of an example 1 is applied and IC36 for microwave as shown in drawing 22 is produced. In this IC, the microstrip line 38 which makes a metal layer a gland with the HBTIC part 37 formed in the shape of an island is formed during production actuation.
[0040]
[Effect of the Invention] Parasitic capacitance is small, it becomes possible to produce the high semiconductor device of dependability and thermal resistance with high productive efficiency, the design change of the semiconductor device to produce can be performed easily, and the applicable range is wide.

[Translation done.]

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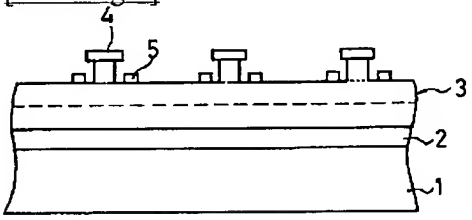
DRAWINGS

[Drawing 1]



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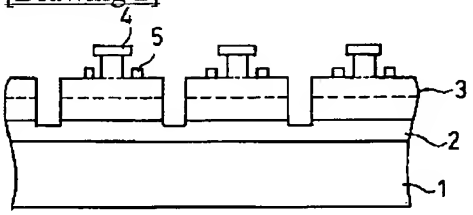

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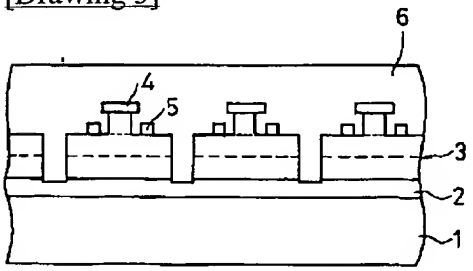

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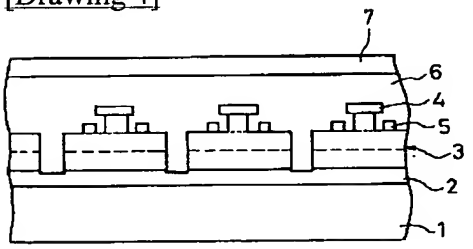

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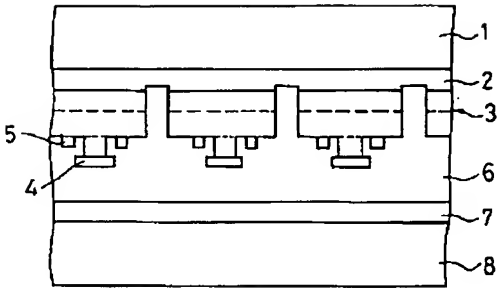

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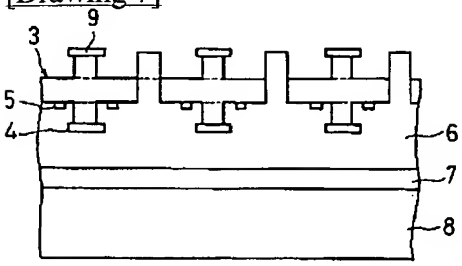

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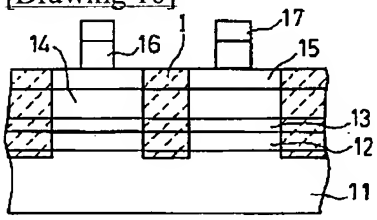

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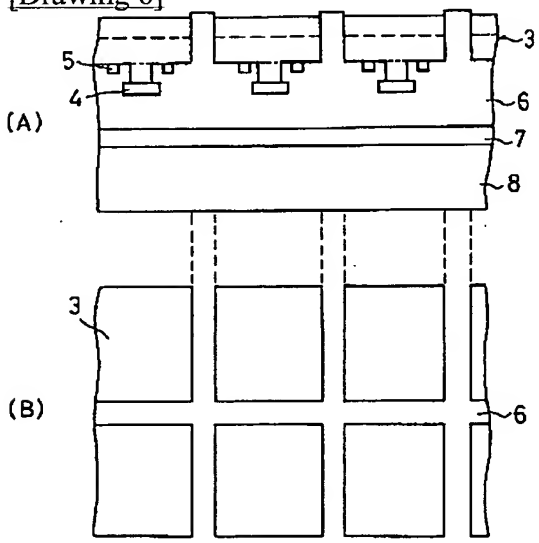

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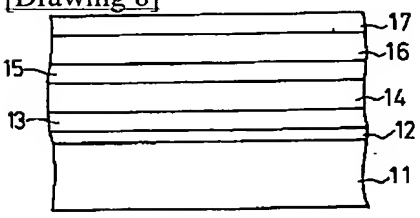

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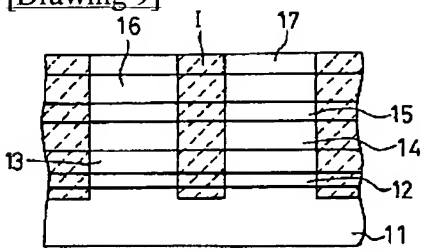
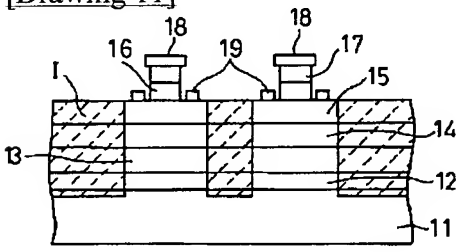


[Drawing 11]



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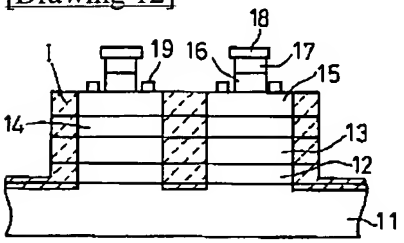

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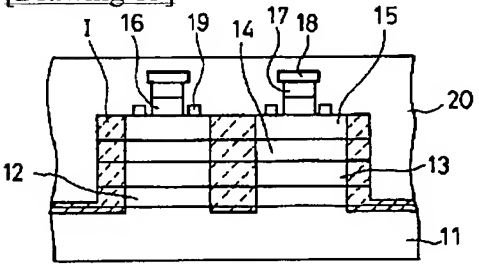

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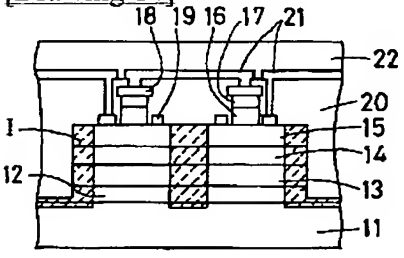

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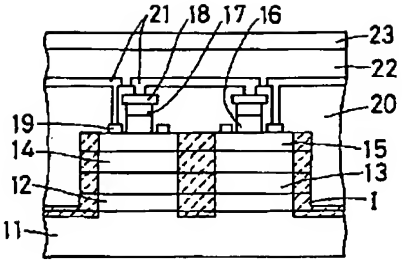

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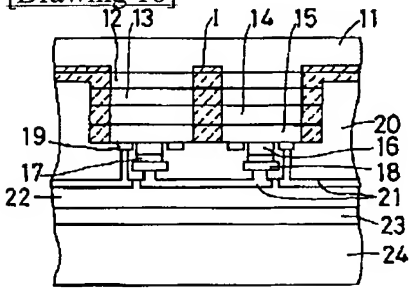

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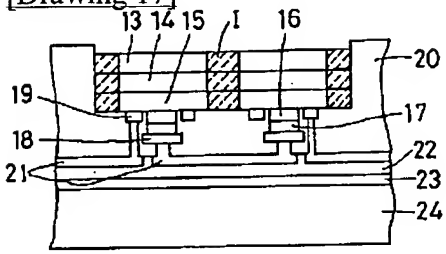

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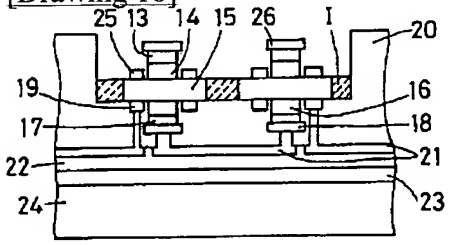

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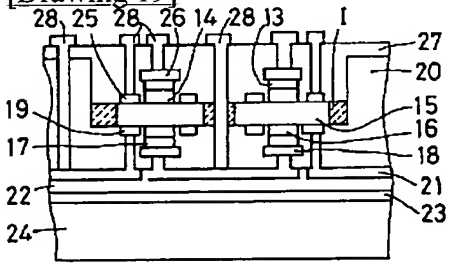
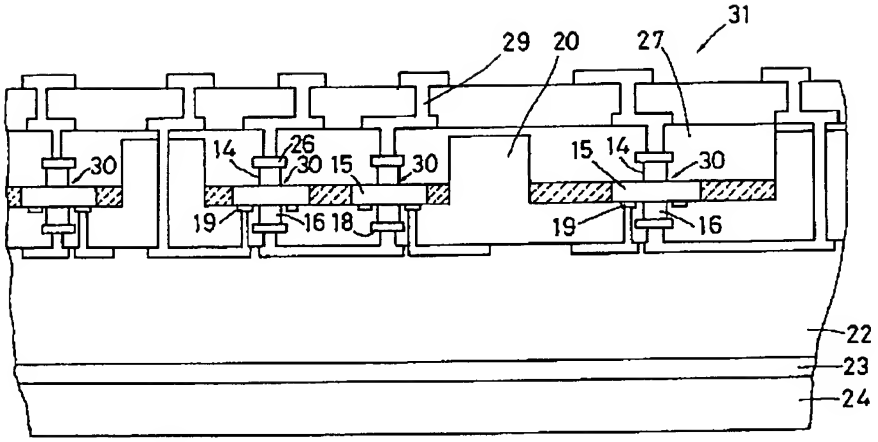
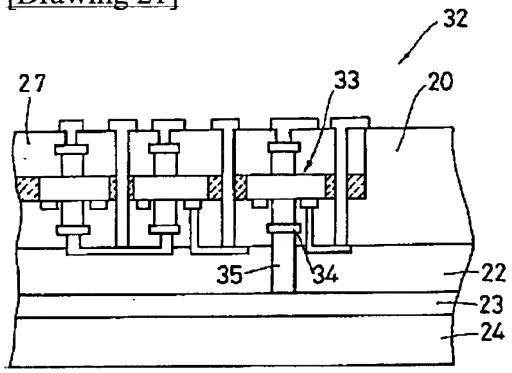


[Drawing 20]



[Drawing 21]



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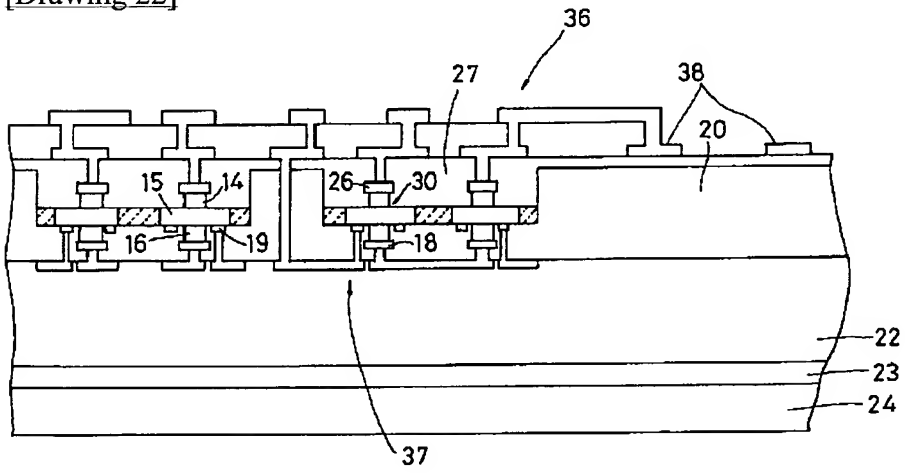

[Translation done.]